UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,757	03/03/2004	Akira Maeda	402989	2915

23548 7590 05/18/2005

LEYDIG VOIT & MAYER, LTD
700 THIRTEENTH ST. NW
SUITE 300
WASHINGTON, DC 20005-3960

EXAMINER	
NOVACEK, CHRISTY L	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,757	MAEDA ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *March 3, 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the preliminary amendment filed March 3, 2004.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: "19", as shown in Figure 1B. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parrish et al. (US 6,550,665) in view of Mertol et al. (US 6,818,996).

Regarding claim 1, Parrish discloses a semiconductor device substrate having a metal electrode thereon that includes a first and second metallic layer lying from an outermost surface of the metal electrode toward the substrate in this order, such that the first metallic layer (220) has tin as a principal constituent and the second metallic layer (230) includes a metallic element which produces a eutectic reaction with tin and the melting point of the first layer is higher than the melting point of the second layer (col. 4, ln. 59 – col. 7, ln. 5). Parrish does not specifically disclose that the metal electrode is built on a wire. Mertol discloses that it is conventional in the art for an integrated circuit to have the semiconductor devices within the circuit electrically connected to wiring, which is in turn connected to metal electrodes that are used to provide electrical connections between the integrated circuit and the circuit board or other upper level device that the integrated circuit is to be connected to (col. 1, ln. 15-45). At the time of the invention, it would have been obvious to one of ordinary art to build the metal electrode of Parrish on a wire because, as is taught by Mertol, it is conventional in the art to provide wiring within the integrated circuit to electrically connect the semiconductor devices on the substrate with the electrode pads that will provide connections to upper level devices.

Regarding claim 2, Parrish discloses that the metallic element that produces the eutectic reaction with tin is indium.

Regarding claim 3, Parrish discloses that the temperature at which the metallic element of the second layer produces the eutectic reaction with tin is no higher than 221°C.

Regarding claim 6, Parrish discloses joining a metal electrode located on a substrate to a circuit card having a joining surface of a material which diffuses into tin when heated. The metal electrode includes multiple metallic layers including a first layer and a second layer lying from an outermost surface of the metal electrode toward the substrate in this order, such that the first layer contains tin as a principal constituent, the second layer contains a metallic element which produces an eutectic reaction with tin, and the melting point of the first layer is higher than the melting point of the second layer. Parrish discloses bringing the metal electrode into contact with the joining surface of the circuit card and heating the metal electrode to a temperature at least equal to the lowest one of the temperatures at which a eutectic reaction occurs between the first and second layers, but lower than the melting point of the first layer. Parrish does not specifically disclose that the metal electrode is built on a wire. Mertol discloses that it is conventional in the art for an integrated circuit to have the semiconductor devices within the circuit electrically connected to wiring, which is in turn connected to metal electrodes that are used to provide electrical connections between the integrated circuit and the circuit board or other upper level device that the integrated circuit is to be connected to (col. 1, ln. 15-45). At the time of the invention, it would have been obvious to one of ordinary art to build the metal electrode of Parrish on a wire because, as is taught by Mertol, it is conventional in the art to provide wiring within the integrated circuit to electrically connect the semiconductor devices on the substrate with the electrode pads that will provide connections to upper level devices.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parrish et al. (US 6,550,665) in view of Mertol et al. (US 6,818,996) as applied to claim 1 above, and further in view of Homma et al. (US 6,569,752).

Regarding claim 4, Parrish does not disclose forming third, fourth and fifth metallic layers between the second layer and the wire. Like Parrish, Homma discloses a method of joining a semiconductor substrate having aluminum pads to a circuit card. Homma discloses that laminates of Cu, Au, and Ni can all be used between the aluminum pad and the tin/indium layer to provide a barrier between the tin/indium layer and the aluminum pad (col. 2, ln. 23-49). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use laminates of Cu, Au and Ni to form a barrier layer between the aluminum pad and the tin/indium layers of Parrish, as taught by Homma, because the barrier layer prevents undesirable diffusion of the aluminum and tin/indium molecules.

Regarding claim 5, Parrish discloses that the metal electrodes may be formed by electroless deposition (col. 6, ln. 16-26).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Akamatsu et al. (US 5,611,481) disclose joining together a semiconductor substrate and a circuit board using a first layer of tin and a second layer of indium.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
May 16, 2005

Michael Trinh
Primary Examiner
Art SPE